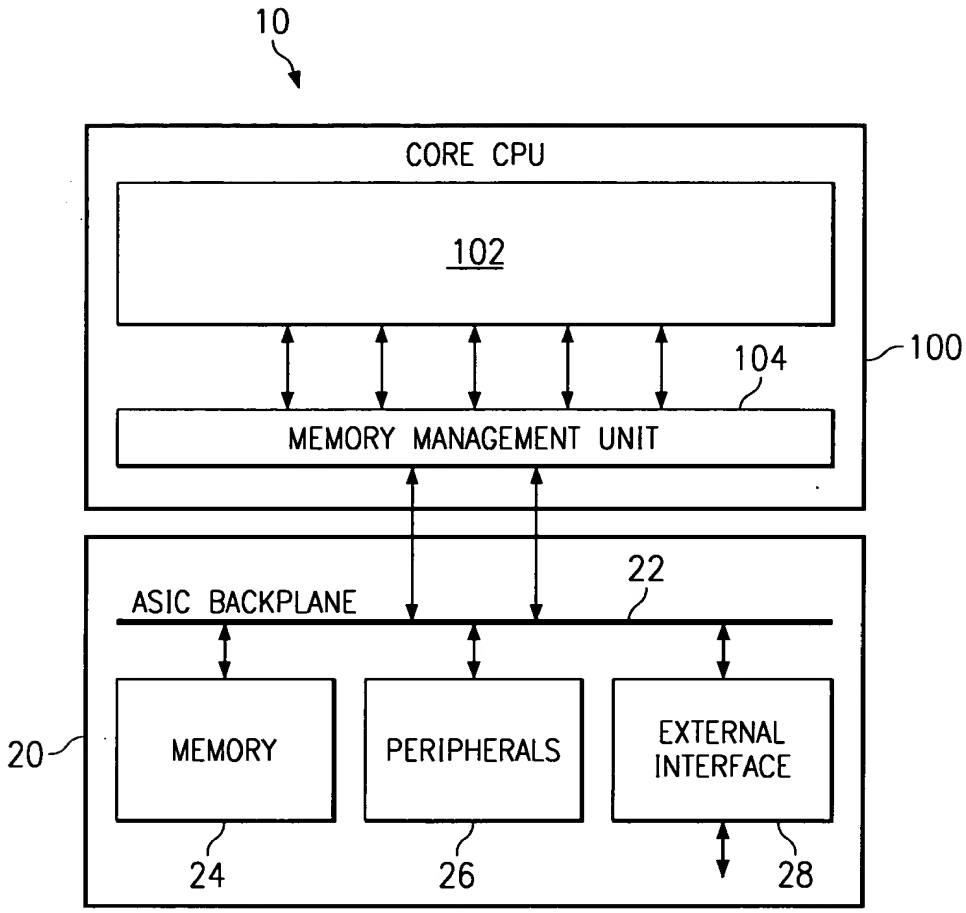

10
CORE CPU
102
104
100
MEMORY MANAGEMENT UNIT
22
ASIC BACKPLANE
20
MEMORY
PERIPHERALS
EXTERNAL INTERFACE
24
26
28

FIG. 1

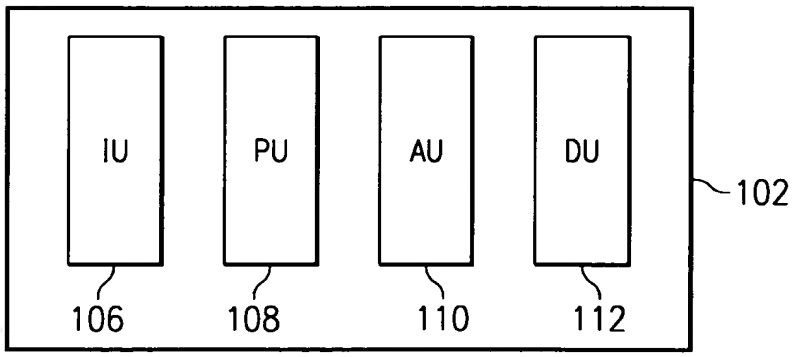

IU
PU
AU
DU
102
106
108
110
112

FIG. 2

0027-6950

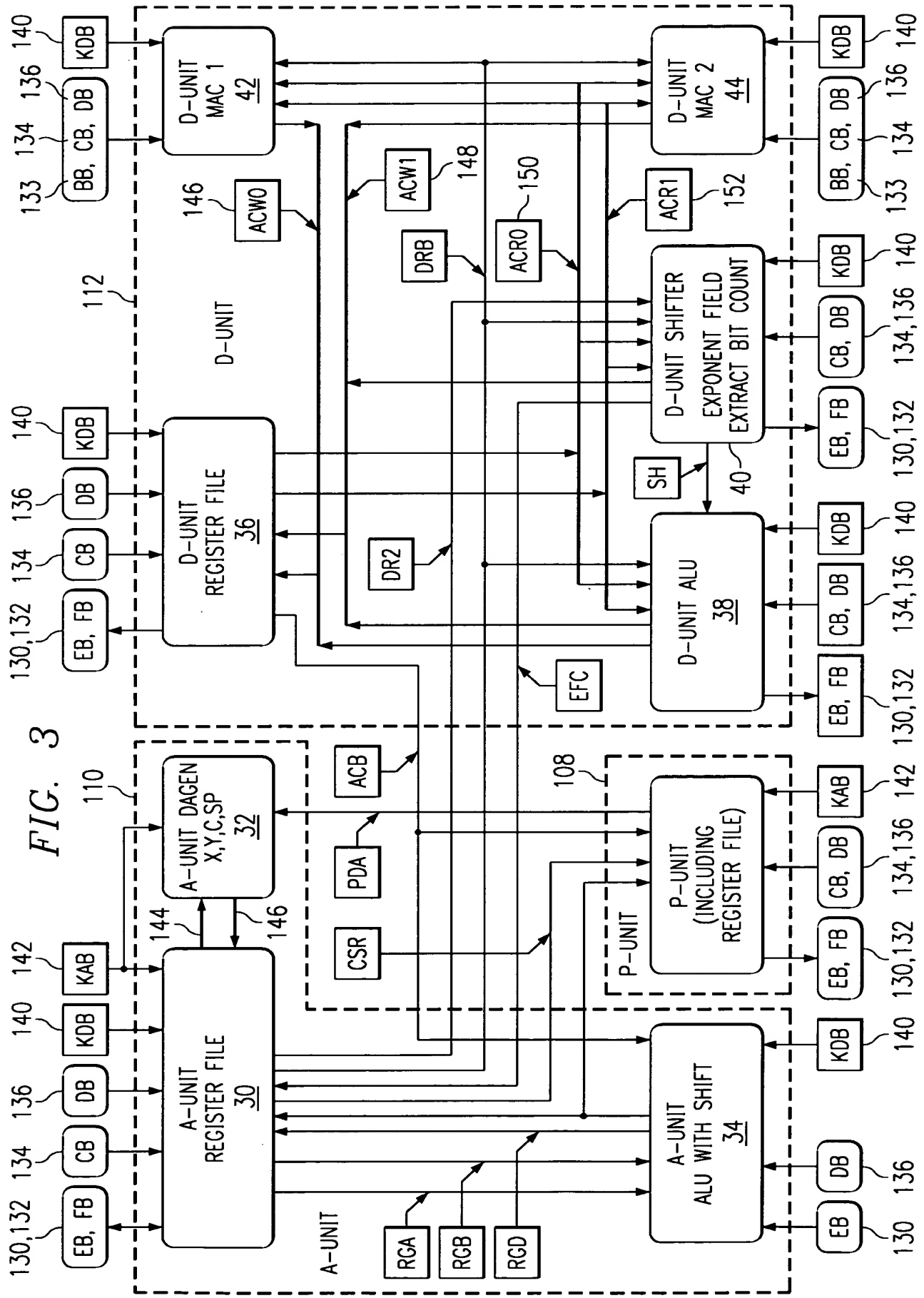


FIG. 3

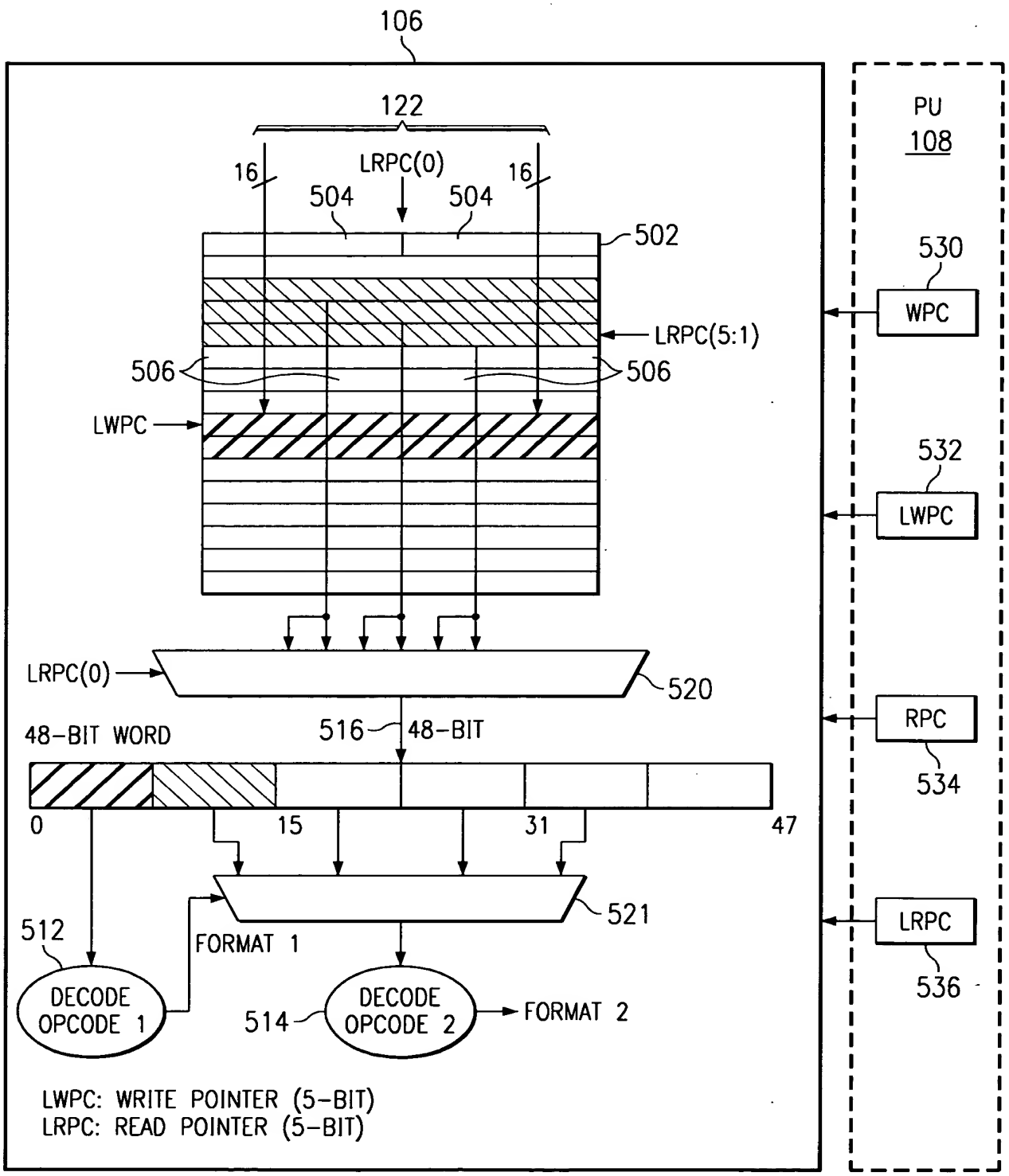

106
122
16
LRPC(0)
16
504
504
502
530
PU
108
WPC
LRPC(5:1)
506
506
LWPC
532
LWPC
LRPC(0)
520
48-BIT WORD
516
48-BIT
RPC
534
0
15
31
47
521
512
FORMAT 1
LRPC
536
DECODE OPCODE 1
514
DECODE OPCODE 2
FORMAT 2
LWPC: WRITE POINTER (5-BIT)
LRPC: READ POINTER (5-BIT)

FIG. 4

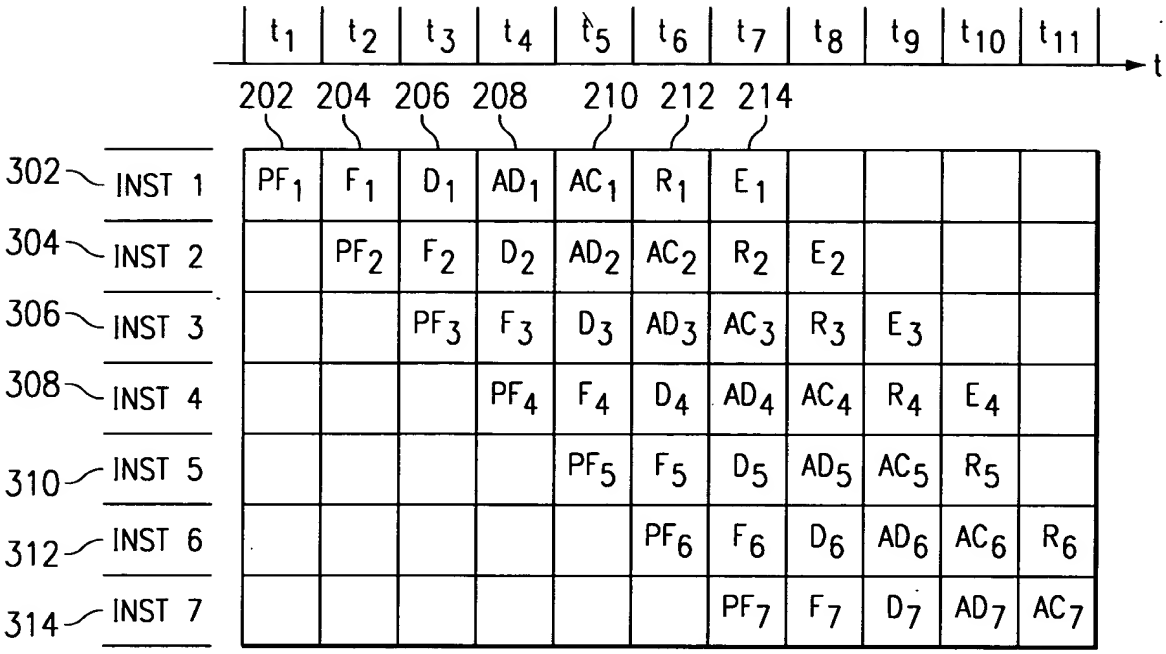


FIG. 5

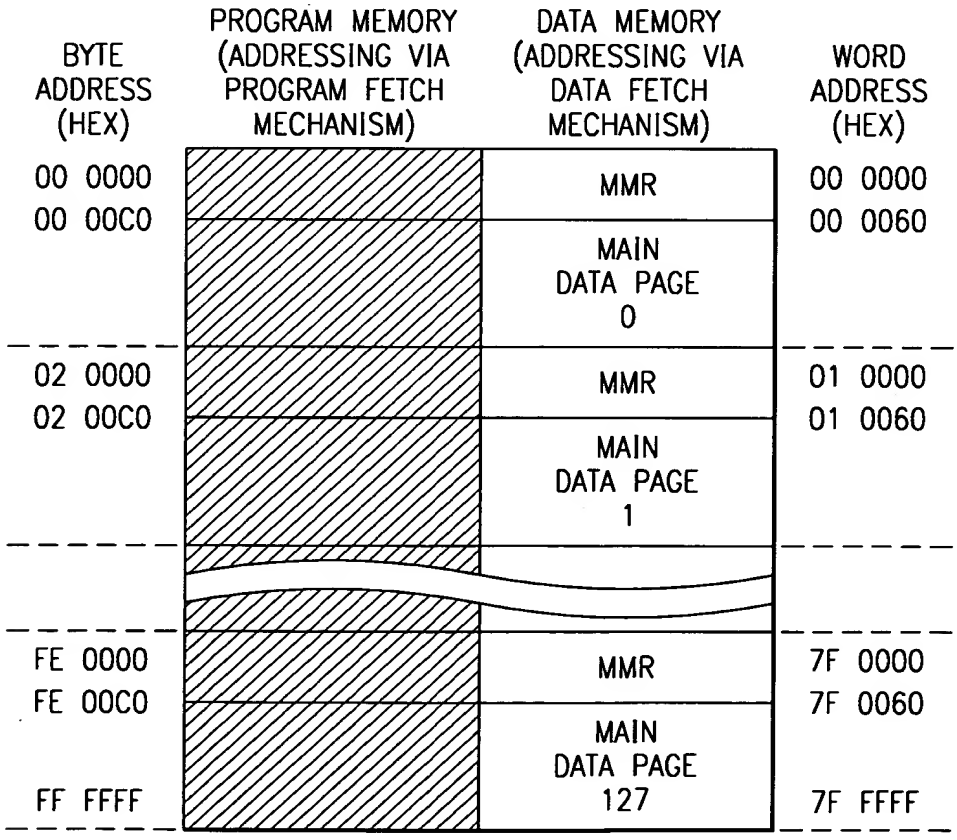


FIG. 7

D0024-E5695-4500

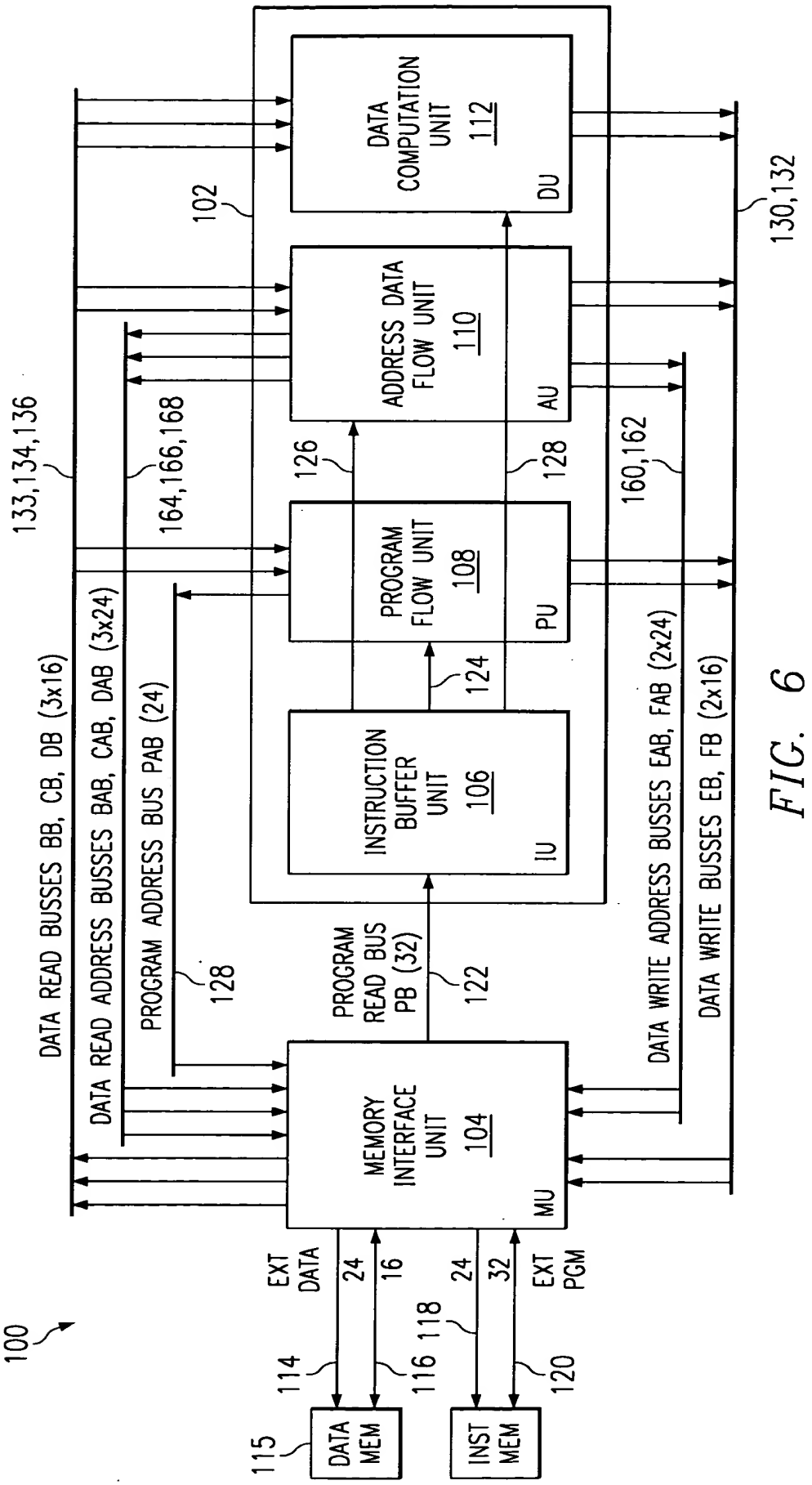

100
DATA READ BUSSES BB, CB, DB (3x16)
DATA READ ADDRESS BUSSES BAB, CAB, DAB (3x24)
PROGRAM ADDRESS BUS PAB (24)
PROGRAM READ BUS PB (32)
DATA WRITE ADDRESS BUSSES EAB, FAB (2x24)
DATA WRITE BUSSES EB, FB (2x16)
133,134,136
164,166,168
102
130,132
160,162
126
128
124
122
128
DATA COMPUTATION UNIT 112
DU
ADDRESS DATA FLOW UNIT 110
AU
PROGRAM FLOW UNIT 108
PU
INSTRUCTION BUFFER UNIT 106
IU
MEMORY INTERFACE UNIT 104
MU
EXT DATA
24
16
24
32
EXT PGM
114
116
118
120
115
DATA MEM
INST MEM

FIG. 6

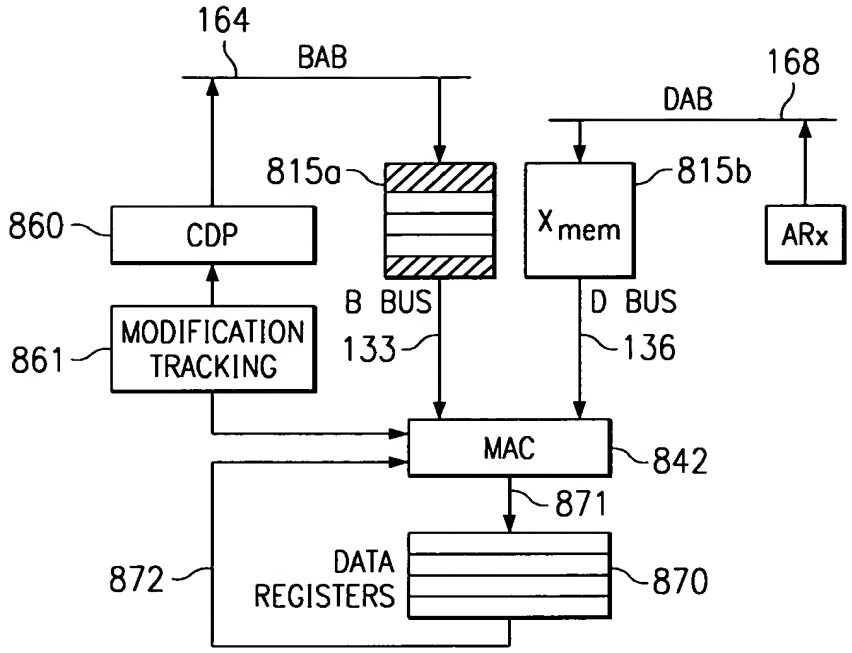

164
BAB
168
DAB
815a
815b
860
CDP
Xmem
ARx
B BUS
D BUS
861
MODIFICATION TRACKING
133
136
MAC
842
871
872
DATA REGISTERS
870

FIG. 8

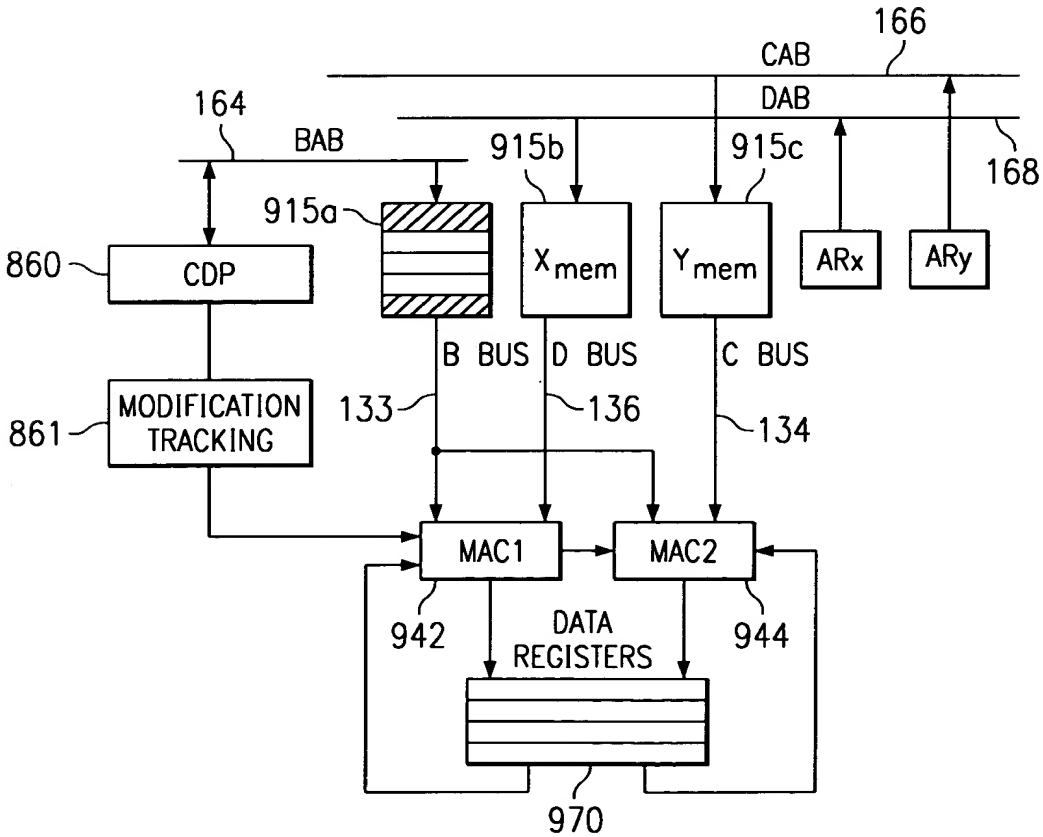

166
CAB
DAB
164
BAB
915b
915c
168
915a
860
CDP
Xmem
Ymem
ARx
ARy
B BUS
D BUS
C BUS
861
MODIFICATION TRACKING
133
136
134
MAC1
MAC2
942
DATA REGISTERS
944
970

FIG. 9

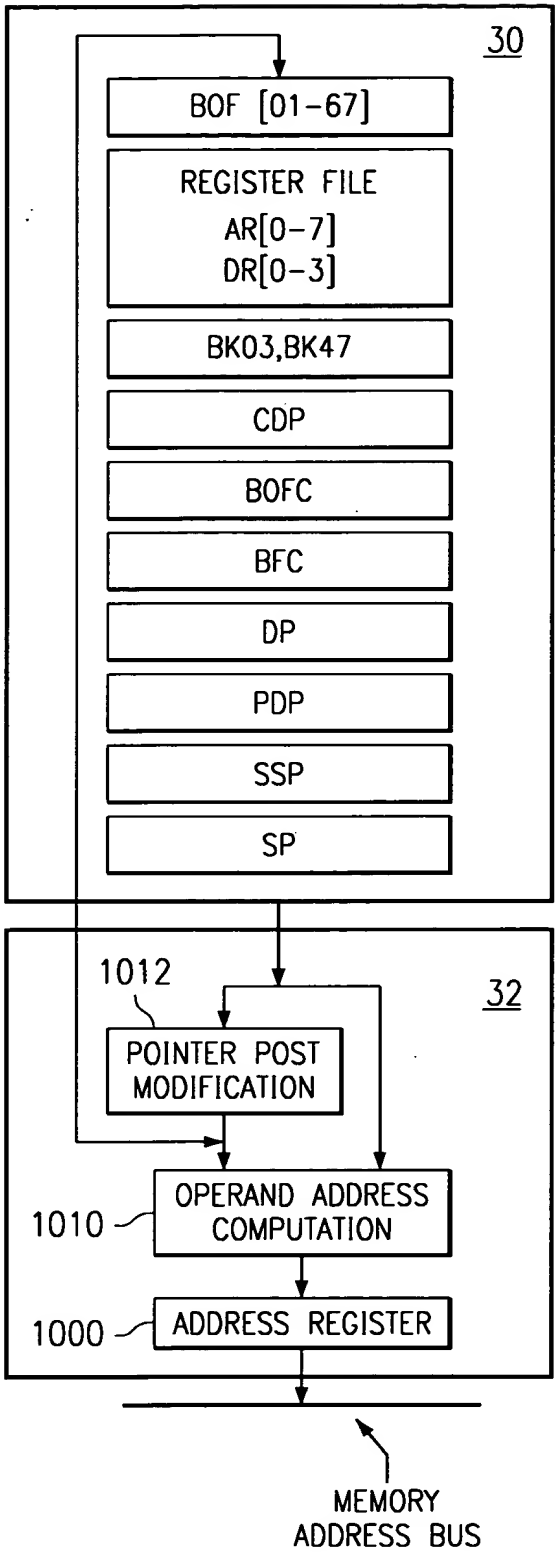


FIG. 10

0002741.3694.2.0

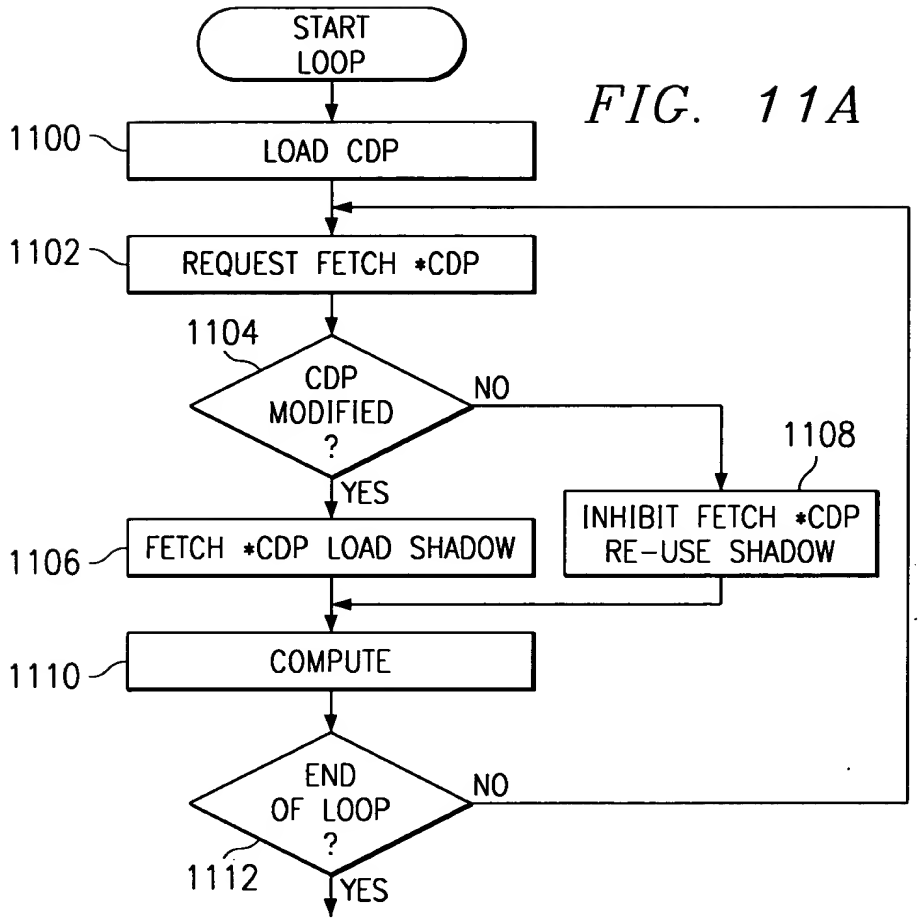
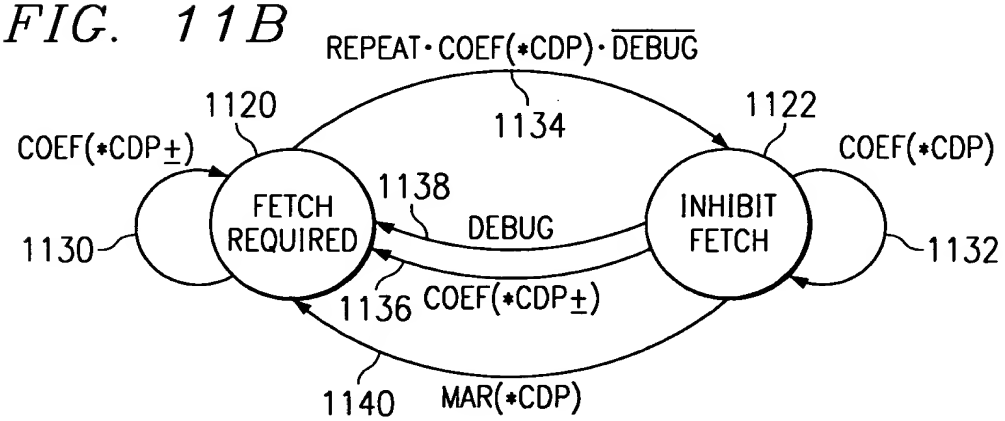


FIG. 11A

FIG. 11B



06/15/98,17:00:00

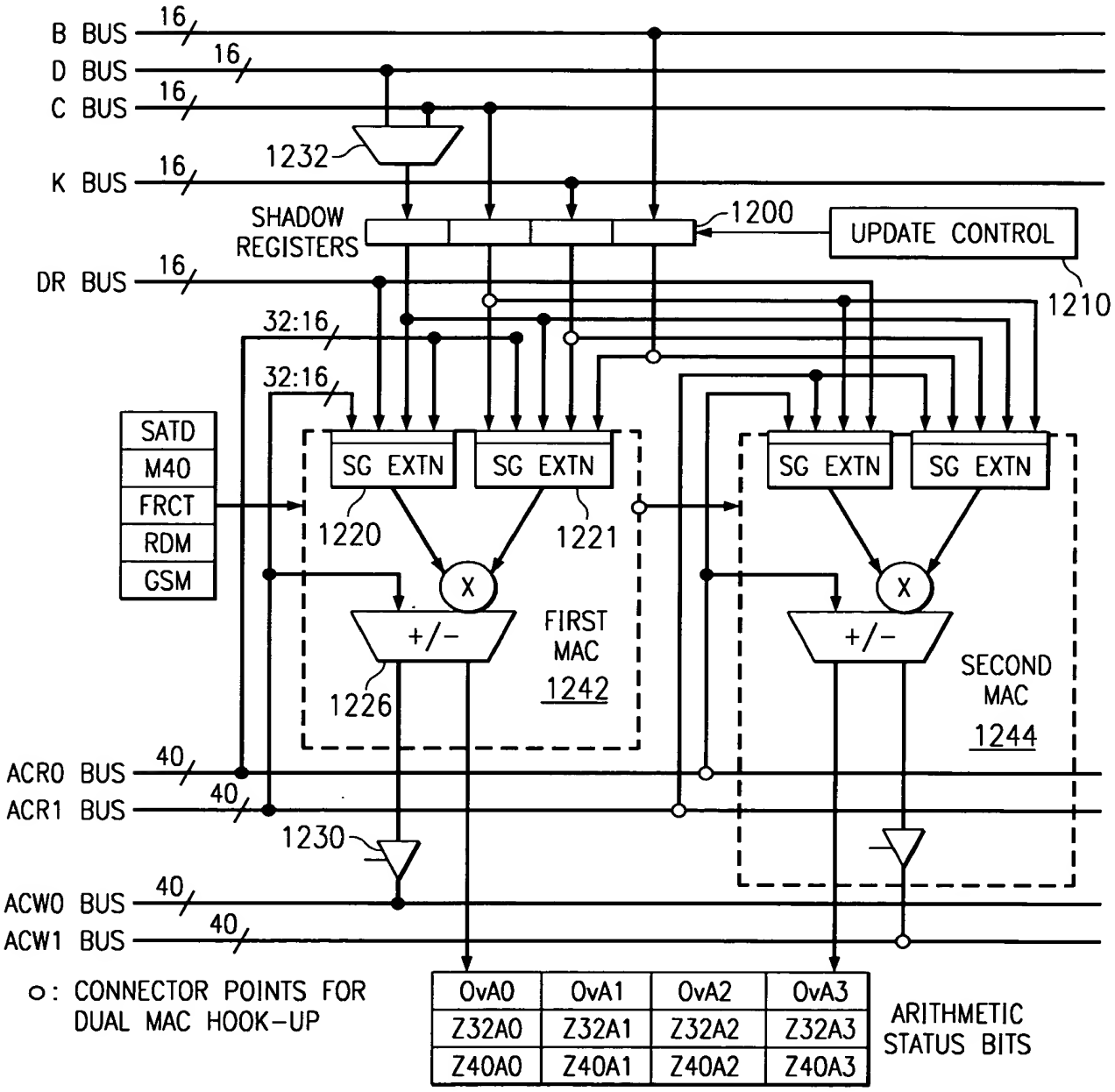

B BUS
D BUS
C BUS
K BUS
DR BUS
ACR0 BUS
ACR1 BUS
ACW0 BUS
ACW1 BUS
16
40
1232
1230
SHADOW REGISTERS
1200
UPDATE CONTROL
1210
32:16
SATD
M40
FRCT
RDM
GSM
SG EXTN
1220
1221
X
+/−
FIRST MAC
1242
1226
SECOND MAC
1244
o: CONNECTOR POINTS FOR DUAL MAC HOOK-UP
OvA0
OvA1
OvA2
OvA3
Z32A0
Z32A1
Z32A2
Z32A3
Z40A0
Z40A1
Z40A2
Z40A3
ARITHMETIC STATUS BITS

FIG. 12

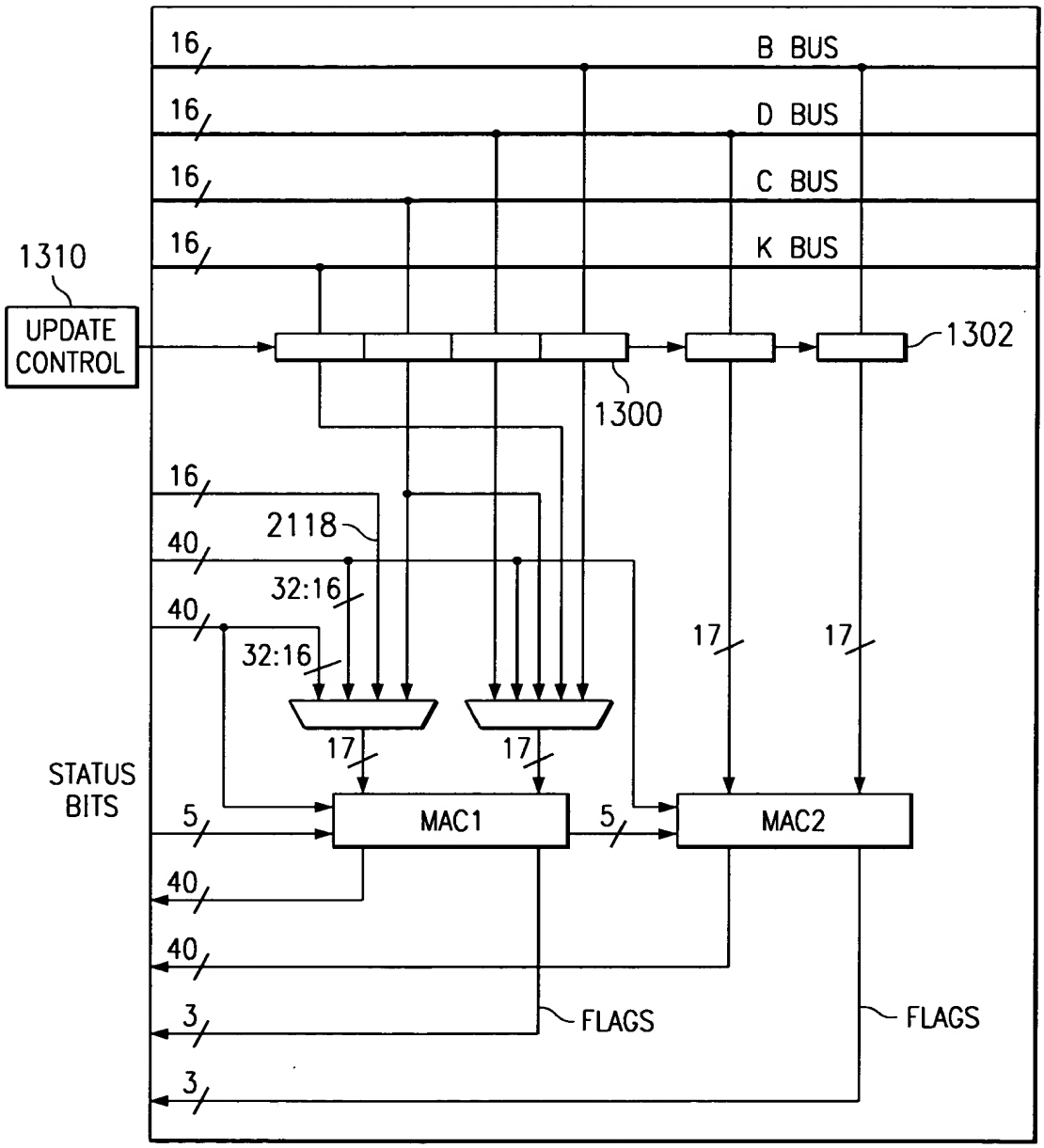


FIG. 13

09754568 - 052601

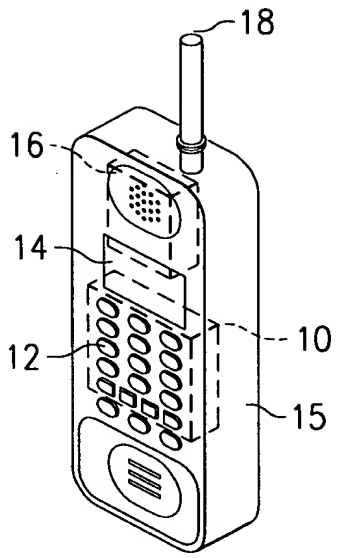
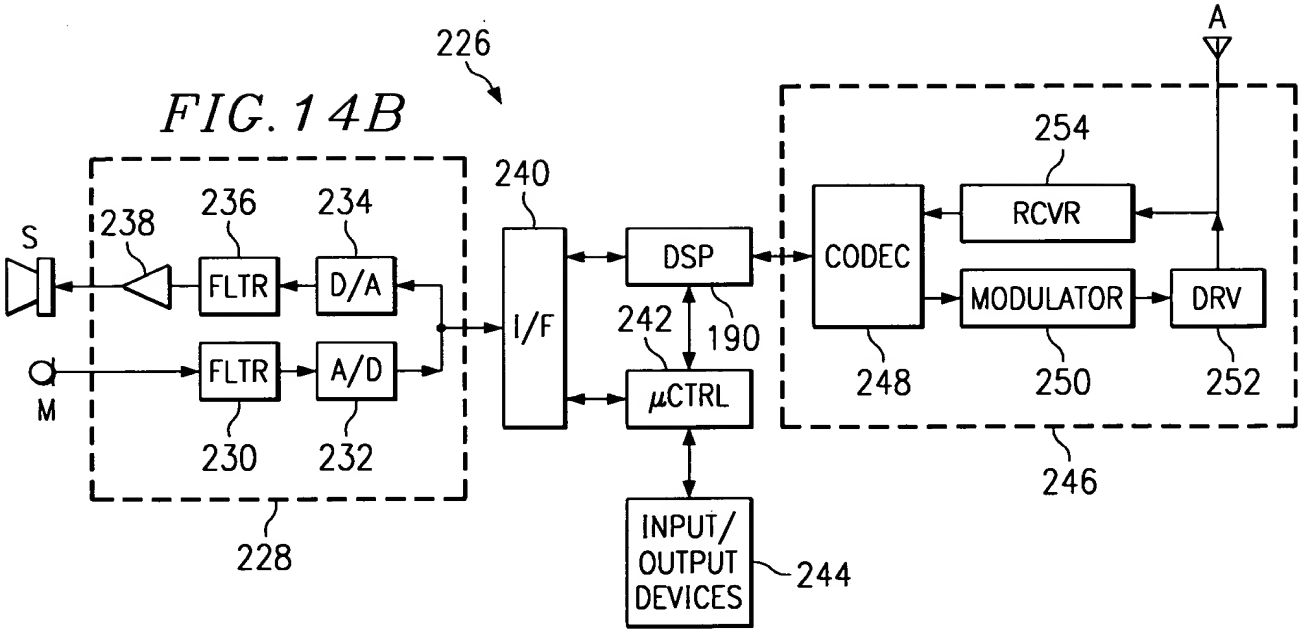


FIG. 14A

FIG. 14B



09/746,493 - 12/20/00